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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/132,157	08/11/1998	LEONARD FORBES	303.229US2	8931

7590 02/26/2002

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EXAMINER
PRENTY, MARK V

ART UNIT	PAPER NUMBER
2822	32

DATE MAILED: 02/26/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
09/132,157	FORBES
Examiner	**Art Unit**
Prenty	2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *three* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Jan 23, 2002* .

2a) ☐ This action is **FINAL.** 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *11, 13, 14, 24-28, 32, and 38-43* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *11, 13, 14, 24-28, 32, and 38-43* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)
16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
18) ☐ Interview Summary (PTO-413) Paper No(s). _____
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other:

This Office Action is in response to the RCE filed January 23, 2002.

The amendment filed November 28, 2001 has been entered.

There is nothing patentable in this application.

Claims 11, 14, 24, 25, 28, 32, 38, 40 and 41 are rejected under 35 U.S.C. §102(b) as anticipated by or, in the alternative, under 35 U.S.C. §103(a) as obvious over Selvakumar et al. (United States Patent 5,426,069, already of record).

With respect to independent claim 11, Selvakumar et al. disclose a p-channel metal-oxide-semiconductor (MOS) transistor, comprising (see the entire patent, particularly column 1, line 51, and the Figs. 1-7 disclosure): a silicon substrate; a silicon dioxide (SiO_2) gate oxide, coupled to the substrate; a gate, coupled to the SiO_2 gate oxide; source/drain regions formed in the substrate on opposite sides of the gate; and a $Si_{1-x}Ge_x$ channel region, having a germanium molar fraction x, located underneath the SiO_2 gate oxide and between the source/drain regions, wherein x is less than or equal to 0.6, and wherein the $Si_{1-x}Ge_x$ channel region forms a continuous $Si_{1-x}Ge_x/SiO_2$ gate oxide interface wherein no germanium oxide is present at the $Si_{1-x}Ge_x/SiO_2$ gate oxide interface (see Fig. 7, as well as column 4, lines 18-19, and column 5, lines 10-11).

The process difference between Selvakumar et al's transistor and claim 11's transistor is that the former's SiGe channel region is formed by implanting germanium into the silicon substrate before the SiO_2 gate oxide is formed, while the latter's SiGe channel region is formed by implanting germanium into the silicon substrate after the SiO_2 gate oxide is formed.

This process difference is not determinative of device claim 11's patentability.

See MPEP §2113.

Claim 11 is thus rejected under 35 U.S.C. §102(b) as anticipated by or, in the alternative, under 35 U.S.C. §103(a) as obvious over Selvakumar et al.

With respect to dependent claim 14, Selvakumar et al's germanium molar fraction is approximately 0.2. See column 3, lines 58-61.

Claim 14 is thus rejected under 35 U.S.C. §102(b) as anticipated by or, in the alternative, under 35 U.S.C. §103(a) as obvious over Selvakumar et al.

With respect to independent claim 24, Selvakumar et al. disclose a p-channel metal-oxide-semiconductor (MOS) transistor formed on a silicon substrate, comprising (see the entire patent, particularly column 1, line 51, and the Figs. 1-7 disclosure): a $Si_{1-x}Ge_x$ channel region, having a germanium molar fraction of x, and formed in the substrate, underneath a silicon dioxide (SiO_2) gate oxide and between a source region and a drain region; wherein x is less than or equal to 0.6, and wherein the $Si_{1-x}Ge_x$ channel region forms a continuous $Si_{1-x}Ge_x/SiO_2$ gate oxide interface wherein no germanium oxide is present at the $Si_{1-x}Ge_x/SiO_2$ gate oxide interface (see Fig. 7, as well as column 4, lines 18-19, and column 5, lines 10-11).

The process difference between Selvakumar et al's transistor and claim 24's transistor is that the former's SiGe channel region is formed by implanting germanium into the silicon substrate before the SiO_2 gate oxide is formed, while the latter's SiGe channel region is formed by implanting germanium into the silicon substrate after the SiO_2 gate oxide is formed.

This process difference is not determinative of device claim 24's patentability. See MPEP §2113.

Claim 24 is thus rejected under 35 U.S.C. §102(b) as anticipated by or, in the

alternative, under 35 U.S.C. §103(a) as obvious over Selvakumar et al.

With respect to independent claim 25, Selvakumar et al. disclose a p-channel metal-oxide-semiconductor (MOS) transistor formed on a silicon substrate, comprising (see the entire patent, particularly column 1, line 51, and the Figs. 1-7 disclosure): a $Si_{1-x}Ge_x$ channel region, having a germanium molar fraction of x, and formed in the substrate, underneath a silicon dioxide (SiO_2) gate oxide and between a source region and a drain region; wherein x is less than or equal to 0.6, and wherein the $Si_{1-x}Ge_x$ channel region forms a continuous $Si_{1-x}Ge_x/SiO_2$ gate oxide interface wherein no germanium oxide is present at the $Si_{1-x}Ge_x/SiO_2$ gate oxide interface (see Fig. 7, as well as column 4, lines 18-19, and column 5, lines 10-11); and wherein the $Si_{1-x}Ge_x$ channel region is formed from ion implanting germanium (Ge) into the substrate at a dose of approximately 2 X 10^{16} atoms/cm^2, and wherein Ge is implanted at an energy of approximately 20 to 100 keV.

The process difference between Selvakumar et al's transistor and claim 25's transistor is that the former's SiGe channel region is formed by implanting germanium into the silicon substrate before the SiO_2 gate oxide is formed, while the latter's SiGe channel region is formed by implanting germanium into the silicon substrate after the SiO_2 gate oxide is formed.

This process difference is not determinative of device claim 25's patentability. See MPEP §2113.

Claim 25 is thus rejected under 35 U.S.C. §102(b) as anticipated by or, in the alternative, under 35 U.S.C. §103(a) as obvious over Selvakumar et al.

With respect to independent claim 28, Selvakumar et al. disclose a p-channel

metal-oxide-semiconductor (MOS) transistor formed on a silicon substrate, comprising (see the entire patent, particularly column 1, line 51, and the Figs. 1-7 disclosure): a $Si_{1-x}Ge_x$ channel region, having a germanium molar fraction of 0.2, and formed in the substrate, underneath a silicon dioxide (SiO_2) gate oxide and between a source region and a drain region; wherein the $Si_{1-x}Ge_x$ channel region forms a continuous $Si_{1-x}Ge_x/SiO_2$ gate oxide interface wherein no germanium oxide is present at the $Si_{1-x}Ge_x/SiO_2$ gate oxide interface (see Fig. 7, as well as column 4, lines 18-19, and column 5, lines 10-11).

The process difference between Selvakumar et al's transistor and claim 28's transistor is that the former's SiGe channel region is formed by implanting germanium into the silicon substrate before the SiO_2 gate oxide is formed, while the latter's SiGe channel region is formed by implanting germanium into the silicon substrate after the SiO_2 gate oxide is formed.

This process difference is not determinative of device claim 28's patentability. See MPEP §2113.

Claim 28 is thus rejected under 35 U.S.C. §102(b) as anticipated by or, in the alternative, under 35 U.S.C. §103(a) as obvious over Selvakumar et al.

With respect to dependent device claim 32, the process recited therein is not determinative of its patentability. Again, see MPEP §2113.

Claim 32 is thus rejected under 35 U.S.C. §102(b) as anticipated by or, in the alternative, under 35 U.S.C. §103(a) as obvious over Selvakumar et al.

With respect to independent claim 38, Selvakumar et al. disclose a semiconductor transistor, comprising (see the entire patent, particularly col. 1, line 51,

and the Figs. 1-7 disclosure): a silicon substrate; a silicon dioxide (SiO_2) gate oxide, coupled to the substrate; a gate, coupled to the SiO_2 gate oxide; source/drain regions formed in the substrate on opposite sides of the gate; and a $Si_{1-x}Ge_x$ channel region, having a germanium molar fraction of x, located underneath the SiO_2 gate oxide and between the source/drain regions, wherein x is less than or equal to 0.6, and wherein the $Si_{1-x}Ge_x$ channel region forms a continuous $Si_{1-x}Ge_x/SiO_2$ gate oxide interface wherein no germanium oxide is present at the $Si_{1-x}Ge_x/SiO_2$ gate oxide interface (see Fig. 7, as well as column 4, lines 18-19, and col. 5, lines 10-11).

The process difference between Selvakumar et al's transistor and claim 38's transistor is that the former's SiGe channel region is formed by implanting germanium into the silicon substrate before the SiO_2 gate oxide is formed, while the latter's SiGe channel region is formed by implanting germanium into the silicon substrate after the SiO_2 gate oxide is formed.

This process difference is not determinative of device claim 38's patentability. See MPEP §2113.

Claim 38 is thus rejected under 35 U.S.C. §102(b) as anticipated by or, in the alternative, under 35 U.S.C. §103(a) as obvious over Selvakumar et al.

With respect to independent claim 40, Selvakumar et al. disclose a semiconductor transistor formed on a silicon substrate, comprising (see the entire patent, particularly column 1, line 51, and the Figs. 1-7 disclosure): a $Si_{1-x}Ge_x$ channel region, having a germanium molar fraction of 0.2 formed in the substrate, underneath a silicon dioxide (SiO_2) gate oxide and between a source region and a drain region; wherein the $Si_{1-x}Ge_x$ channel region forms a continuous $Si_{1-x}Ge_x/SiO_2$

gate oxide interface wherein no germanium oxide is present at the $Si_{1-x}Ge_x/SiO_2$ gate oxide interface (see Fig. 7, as well as column 4, lines 18-19, and col. 5, lines 10-11).

The process difference between Selvakumar et al's transistor and claim 40's transistor is that the former's SiGe channel region is formed by implanting germanium into the silicon substrate before the SiO_2 gate oxide is formed, while the latter's SiGe channel region is formed by implanting germanium into the silicon substrate after the SiO_2 gate oxide is formed.

This process difference is not determinative of device claim 40's patentability. See MPEP §2113.

Claim 40 is thus rejected under 35 U.S.C. §102(b) as anticipated by or, in the alternative, under 35 U.S.C. §103(a) as obvious over Selvakumar et al.

With respect to independent claim 41, Selvakumar et al. disclose a semiconductor transistor formed on a silicon substrate, comprising (see the entire patent, particularly column 1, line 51, and the Figs. 1-7 disclosure): a $Si_{1-x}Ge_x$ channel region, having a germanium molar fraction of x, and formed in the substrate, underneath a silicon dioxide (SiO_2) gate oxide and between a source region and a drain region; wherein x is less than or equal to 0.6, and wherein the $Si_{1-x}Ge_x$ channel region forms a continuous $Si_{1-x}Ge_x/SiO_2$ gate oxide interface wherein no germanium oxide is present at the $Si_{1-x}Ge_x/SiO_2$ gate oxide interface (see Fig. 7, as well as column 4, lines 18-19, and column 5, lines 10-11); and wherein the $Si_{1-x}Ge_x$ channel region is formed from ion implanting germanium (Ge) into the substrate at a dose of approximately 2 X 10^{16} atoms/cm^2, and wherein the Ge is implanted at an energy of approximately 20 to 100 keV.

The process difference between Selvakumar et al's transistor and claim 41's transistor is that the former's SiGe channel region is formed by implanting germanium into the silicon substrate before the SiO_2 gate oxide is formed, while the latter's SiGe channel region is formed by implanting germanium into the silicon substrate after the SiO_2 gate oxide is formed.

This process difference is not determinative of device claim 41's patentability. See MPEP §2113.

Claim 41 is thus rejected under 35 U.S.C. §102(b) as anticipated by or, in the alternative, under 35 U.S.C. §103(a) as obvious over Selvakumar et al.

Claims 13, 26, 27, 39, 42 and 43 are rejected under 35 U.S.C. §103(a) as being unpatentable over Selvakumar et al. (United States Patent 5,426,069, already of record) together with Crabbe' et al. (United States Patent 5,821,577, already of record).

Specifically, the structural difference between Selvakumar et al's transistor (see the entire patent, particularly column 1, line 51, and the Figs. 1-7 disclosure) and the transistor recited in dependent claims 13, 26, 27, 39, 42 and 43 is the former's SiGe channel thickness is unknown, while the latter's SiGe channel thickness is "approximately 100 to 1,000 angstroms" (claims 13, 26, 39 and 42) or "approximately 300 angstroms" (claims 27 and 43).

Crabbe' et al. disclose forming SiGe channels 100 to 500 angstroms thick (see column 6, lines 17-22).

It would have been obvious to one skilled in this art to make Selvakumar et al's SiGe channel of undisclosed thickness 100 to 500 angstroms thick, as suggested by Crabbe' et al.

Claims 13, 26, 27, 39, 42 and 43 are thus rejected under 35 U.S.C. §103(a) as being unpatentable over Selvakumar et al. together with Crabbe' et al.

Claims 11, 14, 24, 25, 28, 32, 38, 40 and 41 are rejected under 35 U.S.C. §102(b) as anticipated by or, in the alternative, under 35 U.S.C. §103(a) as obvious over Nakagawa (newly cited United States Patent 5,272,365).

With respect to independent claim 11, Nakagawa discloses a p-channel metal-oxide-semiconductor (MOS) transistor, comprising (see the entire patent, particularly the Fig. 3 disclosure): a silicon substrate 12; a silicon dioxide (SiO_2) gate oxide "34" (such should be 18, as per Figs. 1-2), coupled to the substrate; a gate 22, coupled to the SiO_2 gate oxide; source/drain regions 14/16 formed in the substrate on opposite sides of the gate; and a $Si_{1-x}Ge_x$ channel region 42, having a germanium molar fraction x, located underneath the SiO_2 gate oxide and between the source/drain regions, wherein x is less than or equal to 0.6, and wherein the $Si_{1-x}Ge_x$ channel region forms a continuous $Si_{1-x}Ge_x/SiO_2$ gate oxide interface wherein no germanium oxide is present at the $Si_{1-x}Ge_x/SiO_2$ gate oxide interface.

The process difference between Nakagawa's transistor and claim 11's transistor is that the former's SiGe channel region is formed by implanting germanium into the silicon substrate before the SiO_2 gate oxide 18 is formed, while the latter's SiGe channel region is formed by implanting germanium into the silicon substrate after the SiO_2 gate oxide is formed.

This process difference is not determinative of device claim 11's patentability. See MPEP §2113.

Claim 11 is thus rejected under 35 U.S.C. §102(b) as anticipated by or, in the

alternative, under 35 U.S.C. §103(a) as obvious over Nakagawa.

With respect to dependent claim 14, Nakagawa's germanium molar fraction is approximately 0.2. See column 3, lines 21-25.

Claim 14 is thus rejected under 35 U.S.C. §102(b) as anticipated by or, in the alternative, under 35 U.S.C. §103(a) as obvious over Nakagawa.

With respect to independent claim 24, Nakagawa discloses a p-channel metal-oxide-semiconductor (MOS) transistor formed on a silicon substrate, comprising (see the entire patent, particularly the Fig. 3 disclosure): a $Si_{1-x}Ge_x$ channel region 42, having a germanium molar fraction of x, and formed in the substrate 12, underneath a silicon dioxide (SiO_2) gate oxide "34" (such should be 18, as per Figs. 1-2) and between a source region 14 and a drain region 16; wherein x is less than or equal to 0.6, and wherein the $Si_{1-x}Ge_x$ channel region forms a continuous $Si_{1-x}Ge_x/SiO_2$ gate oxide interface wherein no germanium oxide is present at the $Si_{1-x}Ge_x/SiO_2$ gate oxide interface.

The process difference between Nakagawa's transistor and claim 24's transistor is that the former's SiGe channel region is formed by implanting germanium into the silicon substrate before the SiO_2 gate oxide 18 is formed, while the latter's SiGe channel region is formed by implanting germanium into the silicon substrate after the SiO_2 gate oxide is formed.

This process difference is not determinative of device claim 24's patentability. See MPEP §2113.

Claim 24 is thus rejected under 35 U.S.C. §102(b) as anticipated by or, in the alternative, under 35 U.S.C. §103(a) as obvious over Nakagawa.

With respect to independent claim 25, Nakagawa discloses a p-channel metal-

oxide-semiconductor (MOS) transistor formed on a silicon substrate, comprising (see the entire patent, particularly the Fig. 3 disclosure): a $Si_{1-x}Ge_x$ channel region 42, having a germanium molar fraction of x, and formed in the substrate 12, underneath a silicon dioxide (SiO_2) gate oxide "34" (such should be 18, as per Figs. 1-2) and between a source region 14 and a drain region 16; wherein x is less than or equal to 0.6, and wherein the $Si_{1-x}Ge_x$ channel region forms a continuous $Si_{1-x}Ge_x/SiO_2$ gate oxide interface wherein no germanium oxide is present at the $Si_{1-x}Ge_x/SiO_2$ gate oxide interface; and wherein the $Si_{1-x}Ge_x$ channel region is formed from ion implanting germanium (Ge) into the substrate.

There are two process differences between Nakagawa's transistor and claim 25's transistor. First, Nakagawa's SiGe channel region is formed by implanting germanium into the silicon substrate before the SiO_2 gate oxide is formed, while claim 25's SiGe channel region is formed by implanting germanium into the silicon substrate after the SiO_2 gate oxide is formed. Furthermore, claim 25 recites a particular implantation dose and energy (Nakagawa is silent in this regard).

These process differences are not determinative of device claim 25's patentability. See MPEP §2113.

Claim 25 is thus rejected under 35 U.S.C. §102(b) as anticipated by or, in the alternative, under 35 U.S.C. §103(a) as obvious over Nakagawa.

With respect to independent claim 28, Nakagawa discloses a p-channel metal-oxide-semiconductor (MOS) transistor formed on a silicon substrate, comprising (see the entire patent, particularly the Fig. 3 disclosure): a $Si_{1-x}Ge_x$ channel region 42, having a germanium molar fraction of 0.2, and formed in the substrate 12, underneath

a silicon dioxide (SiO_2) gate oxide "34" (such should be 18, as per Figs. 1-2) and between a source region 14 and a drain region 16; wherein the $Si_{1-x}Ge_x$ channel region forms a continuous $Si_{1-x}Ge_x/SiO_2$ gate oxide interface wherein no germanium oxide is present at the $Si_{1-x}Ge_x/SiO_2$ gate oxide interface.

The process difference between Nakagawa's transistor and claim 28's transistor is that the former's SiGe channel region is formed by implanting germanium into the silicon substrate before the SiO_2 gate oxide is formed, while the latter's SiGe channel region is formed by implanting germanium into the silicon substrate after the SiO_2 gate oxide is formed.

This process difference is not determinative of device claim 28's patentability. See MPEP §2113.

Claim 28 is thus rejected under 35 U.S.C. §102(b) as anticipated by or, in the alternative, under 35 U.S.C. §103(a) as obvious over Nakagawa.

With respect to dependent device claim 32, the process recited therein is not determinative of its patentability. Again, see MPEP §2113.

Claim 32 is thus rejected under 35 U.S.C. §102(b) as anticipated by or, in the alternative, under 35 U.S.C. §103(a) as obvious over Nakagawa.

With respect to independent claim 38, Nakagawa discloses a semiconductor transistor, comprising (see the entire patent, particularly the Fig. 3 disclosure): a silicon substrate 12; a silicon dioxide (SiO_2) gate oxide "34" (such should be 18, as per Figs. 1-2), coupled to the substrate 12; a gate 22, coupled to the SiO_2 gate oxide; source/drain regions 14/16 formed in the substrate on opposite sides of the gate; and a $Si_{1-x}Ge_x$ channel region 42, having a germanium molar fraction of x, located

underneath the SiO_2 gate oxide and between the source/drain regions, wherein x is less than or equal to 0.6, and wherein the $Si_{1-x}Ge_x$ channel region forms a continuous $Si_{1-x}Ge_x/SiO_2$ gate oxide interface wherein no germanium oxide is present at the $Si_{1-x}Ge_x/SiO_2$ gate oxide interface.

The process difference between Nakagawa's transistor and claim 38's transistor is that the former's SiGe channel region is formed by implanting germanium into the silicon substrate before the SiO_2 gate oxide is formed, while the latter's SiGe channel region is formed by implanting germanium into the silicon substrate after the SiO_2 gate oxide is formed.

This process difference is not determinative of device claim 38's patentability. See MPEP §2113.

Claim 38 is thus rejected under 35 U.S.C. §102(b) as anticipated by or, in the alternative, under 35 U.S.C. §103(a) as obvious over Nakagawa.

With respect to independent claim 40, Nakagawa discloses a semiconductor transistor formed on a silicon substrate, comprising (see the entire patent, particularly the Fig. 3 disclosure): a $Si_{1-x}Ge_x$ channel region 42, having a germanium molar fraction of 0.2 formed in the substrate 12, underneath a silicon dioxide (SiO_2) gate oxide "34" (such should be 18, as per Figs. 1-2) and between a source region 14 and a drain region 16; wherein the $Si_{1-x}Ge_x$ channel region forms a continuous $Si_{1-x}Ge_x/SiO_2$ gate oxide interface wherein no germanium oxide is present at the $Si_{1-x}Ge_x/SiO_2$ gate oxide interface.

The process difference between Nakagawa's transistor and claim 40's transistor is that the former's SiGe channel region is formed by implanting germanium

into the silicon substrate before the SiO_2 gate oxide is formed, while the latter's SiGe channel region is formed by implanting germanium into the silicon substrate after the SiO_2 gate oxide is formed.

This process difference is not determinative of device claim 40's patentability. See MPEP §2113.

Claim 40 is thus rejected under 35 U.S.C. §102(b) as anticipated by or, in the alternative, under 35 U.S.C. §103(a) as obvious over Nakagawa.

With respect to independent claim 41, Nakagawa discloses a semiconductor transistor formed on a silicon substrate, comprising (see the entire patent, particularly the Fig. 3 disclosure): a $Si_{1-x}Ge_x$ channel region 42, having a germanium molar fraction of x, and formed in the substrate 12, underneath a silicon dioxide (SiO_2) gate oxide "34" (such should be 18, as per Figs. 1-2) and between a source region 14 and a drain region 16; wherein x is less than or equal to 0.6, and wherein the $Si_{1-x}Ge_x$ channel region forms a continuous $Si_{1-x}Ge_x/SiO_2$ gate oxide interface wherein no germanium oxide is present at the $Si_{1-x}Ge_x/SiO_2$ gate oxide interface; and wherein the $Si_{1-x}Ge_x$ channel region is formed from ion implanting germanium (Ge) into the substrate.

There are two process differences between Nakagawa's transistor and claim 41's transistor. First, Nakagawa's SiGe channel region is formed by implanting germanium into the silicon substrate before the SiO_2 gate oxide is formed, while claim 41's SiGe channel region is formed by implanting germanium into the silicon substrate after the SiO_2 gate oxide is formed. Furthermore, claim 41 recites a particular implantation dose and energy (Nakagawa is silent in this regard).

These process differences are not determinative of device claim 41's patentability. See MPEP §2113.

Claim 41 is thus rejected under 35 U.S.C. §102(b) as anticipated by or, in the alternative, under 35 U.S.C. §103(a) as obvious over Nakagawa.

Claims 13, 26, 27, 39, 42 and 43 are rejected under 35 U.S.C. §103(a) as being unpatentable over Nakagawa (newly cited United States Patent 5,272,365) together with Crabbe' et al. (United States Patent 5,821,577, already of record).

Specifically, the structural difference between Nakagawa's transistor (see the entire patent, particularly the Fig. 3 disclosure) and the transistor recited in dependent claims 13, 26, 27, 39, 42 and 43 is the former's SiGe channel thickness is unknown, while the latter's SiGe channel thickness is "approximately 100 to 1,000 angstroms" (claims 13, 26, 39 and 42) or "approximately 300 angstroms" (claims 27 and 43).

Crabbe' et al. disclose forming SiGe channels 100 to 500 angstroms thick (see column 6, lines 17-22).

It would have been obvious to one skilled in this art to make Nakagawa's SiGe channel 42 of undisclosed thickness 100 to 500 angstroms thick, as suggested by Crabbe' et al.

Claims 13, 26, 27, 39, 42 and 43 are thus rejected under 35 U.S.C. §103(a) as being unpatentable over Nakagawa together with Crabbe' et al.

The applicant's argument that "the particular process utilized by Selvakumar inherently will produce germanium oxide along with silicon dioxide (SiO_2) when forming the gate oxide layer of Selvakumar," is not persuasive, for at least two reasons.

First, the Selvakumar et al. patent itself evidences that the Selvakumar et al. process does not "inherently" produce germanium oxide along with silicon dioxide when forming the gate oxide layer. Specifically, Selvakumar et al. disclose "...interface between [the] silicon-dioxide [gate oxide layer] and the SiGe channel region" (col. 4, lines 18-19) and "...the extremely abrupt interface at SiGe-channel/Silicon dioxide" (column 5, lines 10-11).

Furthermore, the applicant fails to provide any evidence to support its argument. Mere attorney argument cannot take the place of evidence. See *In re DeBlauwe*, 736 F.2d 699, 222 USPQ 191 (Fed. Cir. 1984).

The applicant's argument with respect to the rejection based on Selvakumar et al. together with Crabbe' et al. is based on its unpersuasive argument with respect to Selvakumar et al. and thus falls therewith.

There is nothing patentable in this application.

Registered practitioners can telephone examiner Prenty at (703) 308-4939. All other parties should telephone (703) 308-0956.

Mark Prenty
Mark V. Prenty
Primary Examiner